

## CLAIMS:

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. In a feedback equalizer device implementing a filter unit performing convolution operations between filter coefficients and one of a plurality of original discrete digital level values for generating a filter output, a multiplier device for multiplying a discrete digital level value with a filter coefficient for said convolution operation, said device comprising:

decoder device for receiving a discrete digital level value to be multiplied with said filter coefficient, and implementing logic for generating control signals according to said digital level value;

a first sub-multiplication circuit receiving said coefficient and implementing logic for multiplying said filter coefficient by  $+1/-1$  or zero (0) in accordance with a first set of control signals and generating a first intermediate multiplication output result therefrom;

a second first sub-multiplication circuit simultaneously receiving said number and implementing logic for multiplying said filter coefficient  $+1/-1$  or zero (0) in accordance with a second set of control signals and generating a second intermediate output result therefrom;

a third sub-multiplication circuit for shifting bits to effect a multiplication of one of said first or second intermediate output result with a discrete digital value different than any of said original plurality of discrete digital level values, and generating a third intermediate result; and,

24 an accumulator device for adding the results of said third and the other of said first or  
25 second intermediate results to obtain a final multiplication result, whereby said final  
26 multiplication result of said number with said original discrete digital level value is  
27 achieved at a greater speed with less redundancy.

1 2. The multiplier device as claimed in Claim 1, wherein said decision feedback equalizer  
2 is implemented in a communication system for processing signals in accordance with a  
3 ATSC (8-VSB) DTV standard, said plurality of original discrete digital level values  
4 comprising:  $+7/-7$ ,  $+5/-5$ ,  $+3/-3$ , and  $+1/-1$  and represented as a three (3)-bit code signal.

1 3. The multiplier device as claimed in Claim 2, wherein said third sub-multiplication  
2 circuit shifts bits to effect a multiplication of one of said first or second intermediate  
3 output result with a discrete digital value of four (4) or eight (8) in accordance with said  
4 control signals.

1 4. The multiplier device as claimed in Claim 2, wherein said first and second sub-  
2 multiplication circuit comprises an inverter circuit.

1 5. The multiplier device as claimed in Claim 2, wherein said an inverter circuit is  
2 implemented as an XOR circuit.

1 6. The multiplier device as claimed in Claim 2, wherein said accumulator device  
2 comprises a carry save adder device for generating sum and carry results.

1 7. The multiplier device as claimed in Claim 6, wherein said accumulator device further  
2 comprises a ripple adder device for adding said sum and carry results.

1 8. The multiplier device as claimed in Claim 7, wherein said ripple adder device receives  
2 one or more said control signals for bit correcting bits when a multiplication by  $-1$  is  
3 performed according to a first or second control signal step.

1 9. The multiplier device as claimed in Claim 6, further including register for storing a  
2 filter output result for use in said convolution operation, said accumulator device further  
3 adding a stored filter output result with a final multiplication result of a current iteration.

1 10. The multiplier device as claimed in Claim 2, further including device for encoding an  
2 original discrete digital level bit value as a set of bits.

1 11. The multiplier device as claimed in Claim 2, wherein said determined number is an  
2 error signal resulting from a recursive decision feedback filter operation.

1 12. Method for performing multiplication in a decision feedback equalizer device  
2 implementing a filter unit for performing convolution operations between filter  
3 coefficients and one of a plurality of original discrete digital level values, said method  
4 comprising:  
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6 a) decoding a discrete digital level value to be multiplied by a filter coefficient, and  
7 implementing logic for generating control signals according to said digital level value;  
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9 b) performing two parallel operations, each operation including multiplying said filter  
10 coefficient by either  $+1/-1$  in accordance with said control signals for generating two  
11 intermediate results, and, corresponding operations for multiplying a corresponding  
12 intermediate result by  $+1$  or zero (0) in accordance with a control signals and generating  
13 respective first and second intermediate output results in parallel;

14 c) shifting bits to effect a multiplication of one of said first and second intermediate  
15 output result with a discrete digital value different than any of said original plurality of  
16 discrete digital level values, and generating a third intermediate result; and,

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18 d) adding the results of said third and the other of said first or second intermediate results  
19 to obtain a final multiplication result, whereby said final multiplication result of said filter  
20 coefficient with said original discrete digital level value is achieved at a greater speed  
21 with less redundancy.

1 13. The method as claimed in Claim 12, wherein said decision feedback equalizer is  
2 implemented in a communication system for processing signals in accordance with a  
3 ATSC (8-VSB) DTV standard, said plurality of original discrete digital level values  
4 comprising:  $+7/-7$ ,  $+5/-5$ ,  $+3/-3$ , and  $+1/-1$  and represented as a three (3)-bit code signal.

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6 14. The method as claimed in Claim 13, wherein said shifting step d) includes the step of  
7 shifting bits to effect a multiplication of one of said first or second intermediate output  
8 result with a discrete digital value of four (4) or eight (8) in accordance with said control  
9 signals.

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11 15. The method as claimed in Claim 13, wherein said first multiplication steps circuit  
12 comprises performing an inversion of said filter coefficient to be multiplied.

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14 16. The method as claimed in Claim 13, wherein steps b) and c) are performed  
15 simultaneously.

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17 17. The method as claimed in Claim 13, further including the step of storing a filter output  
18 result in a register for use during said convolution operation in said filter, said adding step e)

including adding said stored filter output result with a final multiplication result of a current iteration to obtain a new filter output value.

18. A multiplier device for multiplying one of a set of discrete digital level values with a filter coefficient comprising:

decoder device for receiving a discrete digital level value to be multiplied and generating control signals according to said digital level value;

inverter circuit providing two parallel operations, each operation including multiplying said determined number by either +1/-1 in accordance with said control signals for generating two intermediate results;

multiplier circuit receiving said two intermediate results and providing respective parallel operations for multiplying a corresponding intermediate result of said inverter circuit by +1 or zero (0) in accordance with a control signals and generating respective further intermediate results;

logic circuit for shifting bits of one further intermediate result to effect a multiplication of one said further intermediate output result with a discrete digital level value different than any of said original plurality of discrete digital level values; and,

an accumulator device for adding the results of said logic circuit shift multiplication with the other said further intermediate output result to obtain a final multiplication result.

19. The multiplier device as claimed in Claim 18, for use in a filter device for performing a convolution operation in an adaptive feedback equalizer implemented in a communication system for processing signals in accordance with a ATSC (8-VSB) DTV standard, wherein said plurality of original discrete digital level values comprising: +7/-7, +5/-5, +3/-3, and

5 +1/-1 and said discrete digital level values different than any of said original plurality of  
6 discrete digital level values include four (4) and eight (8) in accordance with said control  
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